

Patent Claims

1. Method for communication between an IC and an external DRAM, where the external DRAM (2) has at least one memory bank (21, 22, 23, 24) and communicates with the IC via at least one channel (6, 7, 8), characterized in that the transmission of memory bank commands is prioritized on the basis of a static priority allocation for commands and a dynamic priority allocation for channels.
2. Method according to Claim 1, characterized in that the static priority allocation for commands involves a 'Burst Terminate' command being given the highest, a 'Read' or 'Write' command being given the second highest, an 'Activate' command being given the third highest and a 'Precharge' command being given the lowest priority.
3. Method according to Claim 1 or 2, characterized in that the dynamic priority allocation for channels involves a channel (6, 7, 8) being given the lowest priority after an command has been sent.
4. Method according to one of Claims 1 to 3, characterized in that the dynamic priority allocation involves one of the channels (6, 7, 8) being given the highest priority in the next clock cycle if it does not have the highest priority in the current clock cycle and another channel (6, 7, 8) sends a command.
5. Method according to one of Claims 1 to 4, characterized in that the dynamic priority allocation may involve one of the channels (6, 7, 8) losing the highest priority only when it can send a command.
6. Method according to one of Claims 1 to 5, characterized in that the channels (6, 7, 8) access

- 14 -

physically separate memory areas in the external DRAM (2).

7. Method according to one of Claims 1 to 5, characterized in that the channels (6, 7, 8) access jointly used memory areas in the external DRAM (2) and the assurance is given that no successive access operations to a jointly used memory area will arise.

8. Method according to one of Claims 1 to 7, characterized in that a network (5) is provided which allows at least one channel (6, 7, 8) to access various memory banks (21, 22, 23, 24).

9. Method according to one of Claims 1 to 8, characterized in that two access operations to a memory bank (21, 22, 23, 24) always have an access operation to another memory bank (21, 22, 23, 24) effected between them.

10. Method according to one of Claims 1 to 9, characterized in that two successive access operations to a memory bank (21, 22, 23, 24) are permitted when they are made to the same row in the memory bank (21, 22, 23, 24).

11. Method according to one of Claims 1 to 10, characterized in that the states of the memory banks (21, 22, 23, 24) are depicted by associated state machines (41, 42, 43, 44).

12. Method according to one of Claims 1 to 11, characterized in that a plurality of DRAM modules are used and a chip enable signal is transmitted in order to select the desired module.

13. Memory controller for an IC with an external DRAM, where the external DRAM has at least one memory bank

- 15 -

and communicates with the IC via at least one channel,
characterized in that it has a command scheduler which
prioritizes the transmission of memory bank commands on
the basis of a static priority allocation for commands
5 and a dynamic priority allocation for channels.

14. Appliance for reading and/or writing to storage
media, characterized in that it uses a method according
to one of Claims 1 to 12 or has a memory controller (1)
10 according to Claim 13.